

**Amendments to the Claims:**

This listing of claims will replace all prior versions and listings of claims in the application.

1-34. (Cancelled)

35. (Currently amended) A method of fabricating a semiconductor structure, the method comprising:

providing a semiconductor substrate;

epitaxially growing a first crystalline layer over the substrate;

planarizing a surface of the first layer; and

epitaxially growing a second crystalline layer over the surface of first layer, wherein the first and second layers are substantially lattice-mismatched with respect to each other.

36. (Previously presented) The method of claim 35, wherein the surface of the first layer is planarized by at least one of chemical-mechanical polishing and ion-beam etching.

37. (Previously presented) The method of claim 35, wherein the first crystalline layer is lattice mismatched with respect to the substrate.

38. (Previously presented) The method of claims 37, wherein the first layer comprises a compositionally-graded relaxed epitaxial region.

39. (Previously presented) The method of claim 35, wherein the second crystalline layer is lattice mismatched with respect to the substrate.

40. (Previously presented) The method of claims 39, wherein the second layer comprises a compositionally-graded relaxed epitaxial region.

41. (Previously presented) The method of claim 39, wherein the semiconductor substrate comprises Si and the second crystalline layer comprises Ge and is substantially free of dislocation pile-ups.

42. (Previously presented) The method of claim 35, wherein the first layer comprises a first compositionally-graded relaxed epitaxial region and a first compositionally-uniform layer.

43. (Previously presented) The method of claim 42, wherein the second layer comprises a second compositionally-graded relaxed epitaxial region and a second compositionally-uniform layer.

44. (Previously presented) The method of claim 43, wherein the first and second compositionally-uniform layers are substantially lattice-mismatched.

45. (Previously presented) The method of claim 43, wherein the substrate comprises silicon, and the first and second compositionally-graded relaxed epitaxial regions and the first and second compositionally-uniform layers comprise a  $\text{Ge}_x\text{Si}_{1-x}$  alloy.

46. (Previously presented) The method of claim 45, wherein prior to planarization, the Ge concentration at the surface of the first layer is approximately 50%.

47. (Previously presented) The method of claim 46, wherein the Ge concentration is greater than about 70%.

48. (Previously presented) The method of claim 45, further comprising planarizing a surface of the second layer.

49. (Previously presented) The method of claim 48, wherein, prior to planarization of the first layer, the Ge concentration at the surface thereof ranges from about 20% to about 35%, and, prior to planarization of the second layer, the Ge concentration at the surface thereof ranges from about 50% to about 70%.

50. (Previously presented) The method of claim 48, further comprising epitaxially growing at least one third crystalline layer over the second layer.

51. (Previously presented) The method of claim 50, further comprising planarizing a surface of the third layer.

52. (Previously presented) The method of claim 45 further comprising incorporating compressive strain in at least one of the graded regions to offset tensile strain incorporated during thermal processing.

53. (Previously presented) The method of claim 52, wherein the step of incorporating compressive strain in at least one of the graded regions comprises decreasing the epitaxial growth temperature as Ge concentration increases therein.

54. (Previously presented) The method of claim 53, wherein the step of incorporating compressive strain comprises epitaxially growing the compositionally-graded  $\text{Ge}_x\text{Si}_{1-x}$  alloy with Ge concentration of:

- (a) 0 to about 35 % at a temperature of about 750°C;
- (b) about 35% to about 75% at a temperature ranging from about 650°C to about 750°C; and
- (c) greater than 75 % at about a temperature of about 550°C.